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Superior Reliability of Gate-All-Around Polycrystalline Silicon Thin-Film Transistors with Vacuum Cavities Next to Gate Oxide Edges

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The electrical characteristics and reliability of n-type gate-all-around (GAA) polycrystalline silicon thin-film transistors (poly-Si TFTs) with vacuum cavities next to the gate oxide edges are investigated. This novel structure is successfully fabricated by spacer formation, partial wet etching of a gate oxide, and *in situ* vacuum encapsulation. The electrical characteristics of the GAA poly-Si TFTs with vacuum cavities are superior to those of traditional GAA poly-Si TFTs because the vacuum cavity serves as an offset region to decrease the leakage current in the OFF state and as a field-induced drain (FID) to sustain the on-current in the ON state. In addition, regardless of whether static or dynamic electrical stress is imposed on these devices, the GAA poly-Si TFTs with vacuum cavities exhibit superior reliability to traditional ones owing to the simultaneous reduction of vertical and lateral electric fields near the drain junction during bias stressing due to the greater equivalent gate oxide thickness on the gate electrode edges.

1. Introduction

Polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted a growing amount of attention for their applications in active matrix flat-panel displays (AMFPDs), memory devices, and three-dimensional (3D) ICs.[1–3] In particular, owing to the feasibility of integrating peripheral driving circuits and internal pixel-switching elements, the system-on-panel (SOP) concept is expected to be realized by further increasing the performance and scaling down the feature sizes of poly-Si TFTs.[4] However, the defect states in the grain boundaries and intra-grains of poly-Si channels greatly affect the electrical characteristics and stability of poly-Si TFTs.[5] It has been reported that poly-Si TFTs with multiple narrow channels can effectively reduce the amount of defect states in the channels, resulting in lower threshold voltage (V_{th}), higher field-effect mobility and ON/OFF current ratio, lower OFF-state leakage current, and superior reliability.[6] Furthermore, for memory and 3D ICs applications, it is necessary to shrink the feature sizes of poly-Si TFTs to achieve advanced performance and high packing density. However, the conventional planar poly-Si TFTs with a short channel suffer from severe short-channel effects (SCEs), such as V_{th} fall-off, larger leakage current and subthreshold swing (SS), and serious drain-induced barrier lowering (DIBL), which greatly impede their application.[7]

Recently, poly-Si TFTs with a multigated structure have been proposed to increase the gate controllability of the channels and to suppress the SCEs and kink effect.[8] For example, by adding side channels, the effective channel width of poly-Si TFTs can be increased by fabricating a gate electrode crossing the gate oxide and several poly-Si channels, which becomes more evident as the number of channels increases.[9] Furthermore, gate-all-around (GAA) poly-Si TFTs with multiple nanowire channels have been proposed and demonstrate excellent electrical characteristics but their reliability has not yet been sufficiently investigated.[10–12] Moreover, the OFF-state leakage current of GAA poly-Si TFTs increases more rapidly than that of conventional planar poly-Si TFTs as the gate voltage decreases for n-type devices.[12] It is well known that the leakage current mechanism in the OFF state is field emission via grain boundary trap states due to a high electric field in the depletion region of a drain.[13] Therefore, planar T-gate poly-Si TFTs, formed by the damascene process[14] or the selective wet etching of stacked Si/Ge[15] or Mo/Al[16] gate electrodes, have been proposed to reduce the OFF-state leakage current and to increase the stability, resulting from decreasing the lateral and vertical electric fields simultaneously via the increased effective thickness of the dielectric layer underneath the gate electrode edges. In this study, we propose GAA poly-Si TFTs with vacuum cavities next to the gate oxide edges, which are successfully fabricated by spacer formation, partial wet etching of a gate oxide, and *in situ* vacuum encapsulation, to improve not only the electrical characteristics but also the reliability of devices under static and dynamic electrical stresses.

2. Experimental Procedure

The detailed process flows of n-type GAA poly-Si TFTs with vacuum cavities next to the gate oxide edges are described as follows. First, 50-nm-thick Si_3N_4 and 300-nm-thick SiO_2, used as etching-stop and sacrificial layers, respectively, are sequentially deposited on an oxidized Si substrate by low-pressure chemical vapor deposition (LPCVD). Afterward, the sacrificial SiO_2 is patterned as several dummy stripes with a 100-nm-thick step by anisotropic reactive ion etching (RIE), and then a 100-nm-thick amorphous Si (a-Si) layer is conformally deposited on the patterned SiO_2 by LPCVD at 550 °C. Because the source and drain pads are essential to be served as the sustaining materials for the nanowire channels, the remaining photoresist of the source and drain pads must overlap the ends of the dummy stripes. Next, the a-Si layer is etched away just 100 nm by transformer-coupled plasma RIE (TCP-RIE); meanwhile, the remaining a-Si spacers beside the dummy stripes, which serve as the nanowire channels, are *in situ* fabricated and automatically connected to both source and drain pads. The nanowire channels are easily formed by a side-wall spacer technique without any advanced lithography system. After that, the a-Si is transformed to poly-Si by solid phase crystallization (SPC) at 600 °C for 24 h.

The novel suspended poly-Si channels are formed by fully etching away the remaining sacrificial SiO_2 with diluted HF

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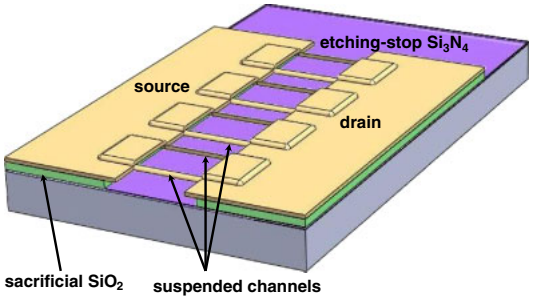
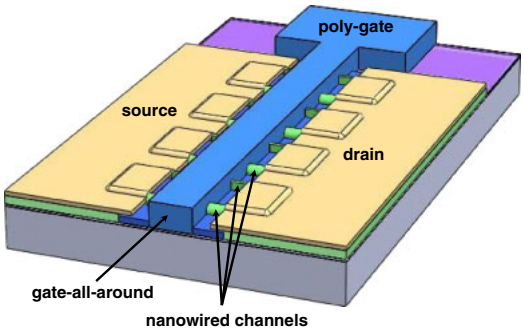
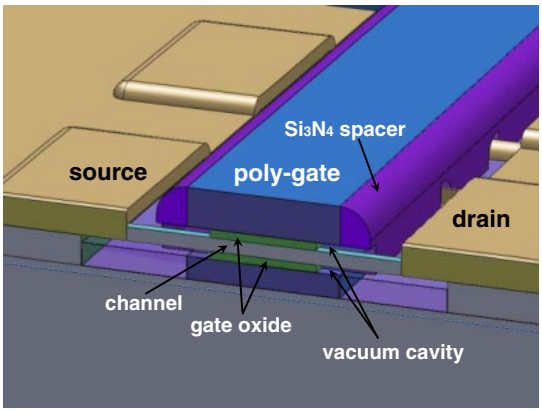


(a)



(b)



(c)

Fig. 1. (Color online) 3D schematic diagrams of the key processes in fabricating GAA poly-Si TFTs with vacuum cavities next to the gate oxide edges: (a) suspended channel formation, (b) GAA poly-gate formation, and (c) vacuum cavity formation.

solution, and the etching process of sacrificial SiO_2 is automatically terminated at the Si_3N_4 etching-stop layer. A 3D schematic diagram of the key process for suspended poly-Si channel formation is shown in Fig. 1(a). A 50-nm-thick tetraethoxysilane (TEOS) gate oxide and a 200-nm-thick *in situ* phosphorus-doped poly-Si gate are sequentially and conformally deposited around the suspended poly-Si nanowires. After the *in situ* doped poly-Si gate is patterned by TCP-RIE, the n^+ source and drain are performed by $^{31}P^+$ self-aligned ion implantation through the gate oxide at a dosage of $5 \times 10^{15}\,cm^{-2}$ and an energy of 62 keV. There is no lightly doped drain (LDD) structure in the GAA poly-Si TFTs. A 3D schematic diagram of the key process for GAA poly-Si gate formation is shown in Fig. 1(b). Next, a 200-nm-thick Si_3N_4 layer is deposited by LPCVD at 790 °C and the dopants are simultaneously activated in this stage. The

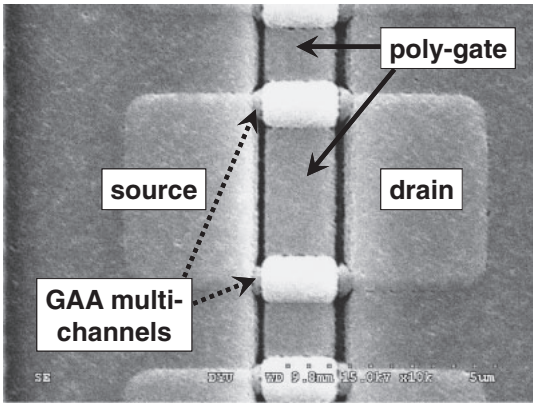


Fig. 2. Top-view SEM image of a GAA poly-Si TFT with multiple nanowire channels and vacuum cavities next to the gate oxide edges.

Si_3N_4 spacers next to the poly-Si gate are formed by the RIE etching-back process without any additional mask. For the GAA poly-Si TFTs with vacuum cavities, the samples are dipped into diluted HF solution ($HF : H_2O = 3 : 50$) for 3 min to etch out the edges of the gate oxide. A 3D schematic diagram of this key process for GAA poly-Si TFTs with vacuum cavities is shown in Fig. 1(c). It demonstrates that a vacuum cavity, which surrounds the nanowire poly-Si channel, is achieved underneath the upper poly-Si gate and above the lower poly-Si gate. The length of a cavity is determined by the etching time and the concentration of the diluted HF solution. Next, a 500-nm-thick SiH_4/N_2O-based oxide film is deposited as a passivated and sealing layer by a PECVD system under a depositing pressure of 1 Torr, and thus *in situ* vacuum cavities are formed next to the gate oxide edges. The main purpose of the Si_3N_4 spacer is to ensure the existing and same length of vacuum cavities from the end of the poly-Si gate electrode toward inside during the passivation oxide deposition even if the outside edges of cavities are partially refilled by this passivation oxide. Finally, after via hole formation, metallization, and gate, drain, and source metal pad definition, NH_3 plasma passivation is performed at 250 °C for 1 h to complete the fabrication process. For comparison, GAA poly-Si TFTs without vacuum cavities are fabricated by the same procedures except the cavity formation process.

3. Results and Discussion

Figure 2 shows a top-view SEM image of GAA poly-Si TFT with multiple nanowire channels and vacuum cavities next to the gate oxide edges. Because the GAA poly-Si TFTs are fabricated by a spacer formation technique, there are two nanowire channels in every dummy stripe. Because the methods used to fabricate the GAA poly-Si TFTs in this study are almost the same as those in Liao *et al.*'s report, the width of a single nanowire channel with a quasi-triangle structure is estimated to be 0.3 μm.[12] Therefore, the channel width of GAA poly-Si TFTs can be determined by the number of nanowire channels. Moreover, the length of the vacuum cavity underneath the poly-Si gate is about 170 nm, which is obtained from a SEM image of a dummy substrate, not shown here. The Si_3N_4 spacer ensures that there is no passivation oxide directly underneath the edge of the gate

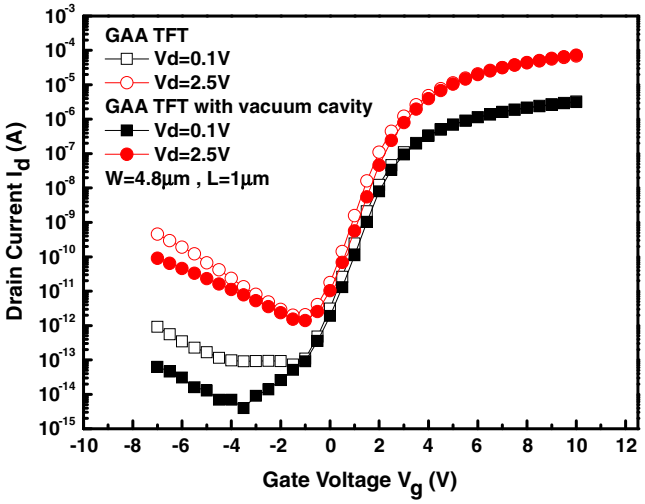


Fig. 3. (Color online) I_d–V_g transfer curves of the GAA poly-Si TFTs with/without vacuum cavities under $V_d = +0.1$ and $+2.5$ V.

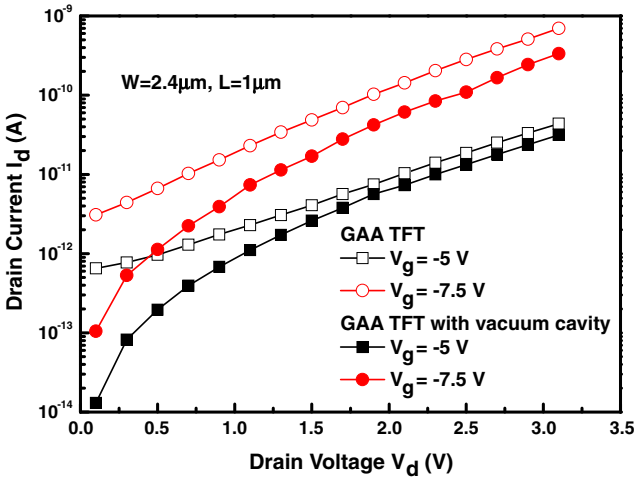


Fig. 4. (Color online) I_d–V_d leakage current characteristics of GAA poly-Si TFTs with/without vacuum cavities in OFF state under applied gate voltages of -5 and -7.5 V.

electrode even if the outside edges of cavities are partially refilled by this passivation oxide. Because the permittivity of a vacuum is 1, the lowest permittivity in nature, and 3.9 for a SiO_2 film, the equivalent oxide thickness of this vacuum cavity is 3.9 times that of the actual gate oxide. The nanowire poly-Si inside the vacuum cavity can be considered as an offset region, and the surrounding poly-Si gate electrode outside the vacuum cavity serves as a field plate so that GAA poly-Si TFTs with vacuum cavities act as field-induced drain (FID) TFTs without any additional subgate bias.

The drain current vs gate voltage (I_d–V_g) transfer curves of GAA poly-Si TFTs with and without vacuum cavities and a channel width (W)/channel length (L) of 4.8/1 μm under $V_d = +0.1$ and $+2.5$ V are illustrated in Fig. 3. Because of the completely surrounding gate structure and the increase in electric field by the spacer channel with three sharp corners, GAA poly-Si TFTs exhibit excellent electrical characteristics, resulting from the improvement of gate controllability in the TFTs with a short channel.[12] Furthermore, the OFF-state leakage current of the GAA poly-Si TFTs with vacuum cavities is significantly lower than that of traditional ones (GAA poly-Si TFTs without vacuum cavities), resulting from the simultaneous reduction of lateral and vertical electric fields near the drain junction due to the greater equivalent gate oxide thickness on the gate electrode edges.[16,17] Moreover, the on-current of the GAA poly-Si TFTs with vacuum cavities in the ON state is almost the same as that of traditional ones owing to the slightly shortened channel length and the FID structure, which can induce a inversion layer in the offset region. The ON/OFF current ratio is defined as the ratio of the ON-state current to the minimum OFF-state leakage current. The ON-state current is defined as I_d at $V_g = +10$ V and $V_d = +2.5$ V, and the minimum leakage current is defined as the minimum I_d at $V_d = +2.5$ V in the I_d–V_g transfer curves. Compared with the traditional GAA poly-Si TFTs, the ON/OFF current ratio of the GAA poly-Si TFTs with vacuum cavities is improved from 3.46×10^7 to 5.19×10^7, resulting from a significant reduction of the OFF-state leakage current and the maintenance of on-current. The V_{th} of the GAA poly-Si TFTs is defined as the V_g corresponding to the normalized drain current of $I_d = (W/L) \times 10$ nA at $V_d = +0.1$ V. It is observed that the V_{th} of the GAA poly-Si TFTs with vacuum cavities is about 2.62 V, slightly larger than that of traditional ones, 2.51 V, resulting from the greater equivalent oxide thickness in the vacuum cavity region.[15] The definition of DIBL is $\Delta V_g/\Delta V_d$ at $I_d = 0.1$ nA.[10] Owing to the nanowire structure and the three sharp corners of the GAA poly-Si channel, GAA poly-Si TFTs with and without vacuum cavities possess a low DIBL effect and the values of DIBL are 0.175 and 0.142 V/V, respectively.

The drain current vs drain voltage (I_d–V_d) OFF-state leakage current characteristics of GAA poly-Si TFTs with and without vacuum cavities and $W/L = 2.4/1$ μm under V_g of -5 and -7.5 V are shown in Fig. 4. It can be observed that the OFF-state leakage currents of the GAA poly-Si TFTs with vacuum cavities are significantly lower than those of traditional ones, especially at a smaller V_d, resulting from the simultaneous reduction of lateral and vertical electric fields near the drain junction due to the greater equivalent gate oxide thickness on the gate electrode edges.[16,17] It is well known that the mechanism of OFF-state leakage current is field emission via grain boundary trap states due to a high electric field in the depletion region of a drain.[13] Therefore, the GAA poly-Si TFTs with vacuum cavities exhibit a lower OFF-state leakage current. Under a fixed V_g bias, however, the difference in leakage current between the GAA poly-Si TFTs with and without vacuum cavities gradually becomes small with increasing V_d bias. In previous reports, it was observed that under the same bias voltages of V_g and V_d for poly-Si TFTs with vacuum gaps[16] or air cavities[17] and conventional ones, the decreased ratio in the vertical electric field is larger than that in the lateral electric field according to the data obtained from the simulation of electric field distributions. Therefore, under fixed V_g and very low V_d, the leakage current in the OFF state is dominated by the vertical electric field, which possesses the biggest difference between GAA poly-Si TFTs with and without vacuum cavities owing to the larger decreased ratio of the vertical electric field. With increasing V_d, the leakage current gradually become

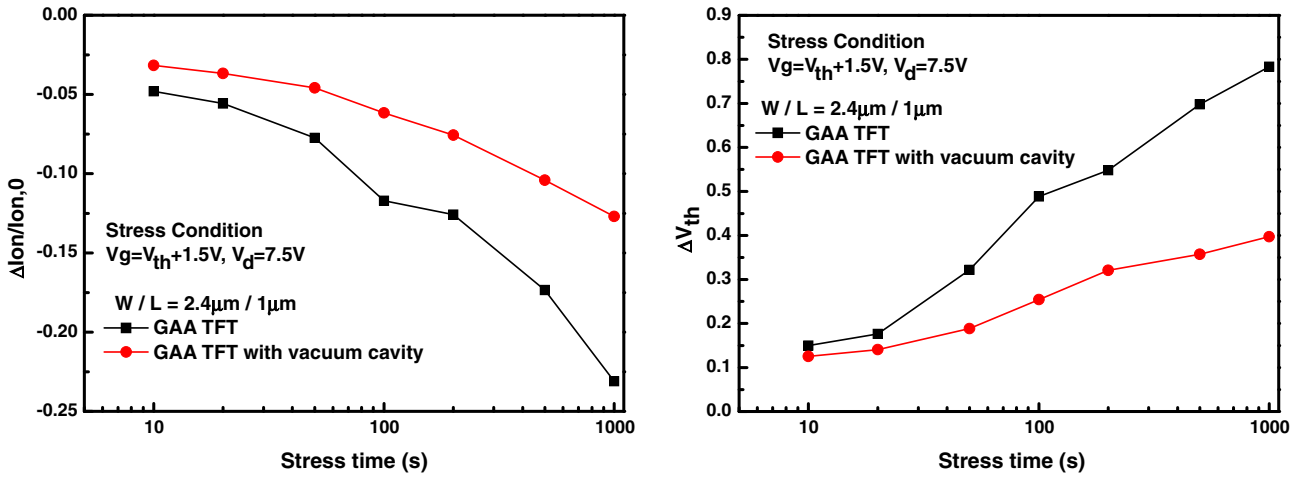


Fig. 5. (Color online) Dependence of (a) I_{on} and (b) V_{th} degradation on the stress time for the GAA poly-Si TFTs with/without vacuum cavities under hot carrier stress condition.

dominated by the lateral electric field and the difference in these leakage currents gradually becomes small owing to the smaller decreased ratio of the lateral electric field. In contrast, compared with those in Fig. 3, for the I_d–V_g transfer curves of GAA poly-Si TFTs with and without vacuum cavities under a fixed V_d bias of +2.5 V with decreasing V_g bias in the OFF state, the difference in the leakage currents between GAA poly-Si TFTs with and without vacuum cavities gradually becomes large, resulting from the more significant reduction ratio of the vertical electric field near the drain junction, which agrees with the simulation data in previous studies.[16,17)]

To investigate the reliability of the GAA poly-Si TFTs with and without vacuum cavities after electrical stress, we examine the on-current (I_{on}) and V_{th} degradation of the devices with $W/L = 2.4/1\,\mu m$. The definition of I_{on} is the I_d corresponding to $V_g = +10$ V and $V_d = +0.1$ V according to the I_d–V_g transfer curves. The degradation of I_{on} is defined as $\Delta I_{on}/I_{on,0}$, where $I_{on,0}$ is the initial I_{on} and ΔI_{on} is the difference between $I_{on,stress}$ (I_{on} after stress) and $I_{on,0}$. The degradation of V_{th} is defined as ΔV_{th}, which is the difference between $V_{th,stress}$ (V_{th} after stress) and $V_{th,0}$ (initial V_{th}). Under electrical stress, the deterioration of poly-Si TFTs is mainly induced by two degradation mechanisms: the hot carrier effect and self-heating effect. The hot carrier effect is principally caused by a high electric field near the drain depletion region,[18,19)] usually at low gate and high drain-stressing voltages, and can be relaxed by an LDD structure.[18)] Because the initial V_{th} of the GAA poly-Si TFTs with and without vacuum cavities is different, we adopt $V_g = V_{th} + 1.5$ V and $V_d = +7.5$ V as the hot carrier stress conditions, and the dependence of I_{on} and V_{th} degradation on the stress time is shown in Fig. 5. Under DC bias stress, the GAA poly-Si TFTs with vacuum cavities simultaneously reduce the lateral and vertical electric fields, resulting from the greater equivalent gate oxide thickness on the gate electrode edges. Therefore, the GAA poly-Si TFTs with vacuum cavities demonstrate better reliability than traditional ones because the vacuum cavity serves as an FID to suppress the hot carrier effect, which is similar to the effect of an LDD structure.[15,17)] On the other hand, the self-heating effect degrades devices owing to the generation of defects at the oxide interface and in the poly-Si channel, resulting from the breaking of Si-H bonds and the regeneration of dangling bonds.[19)] The self-heating effect is also called the Joule heating effect and is caused by a large drain current,[19,20)] generally at both high gate and drain-stressing voltages. Therefore, $V_g = V_{th} + 6.5$ V and $V_d = +8.5$ V are adopted as the self-heating stress conditions, and the dependence of I_{on} and V_{th} degradation on the stress time is shown in Fig. 6. It is observed that the GAA poly-Si TFTs with vacuum cavities have greatly superior reliability to traditional ones, resulting from the reduction of lateral and vertical electric fields during bias stressing. On the basis of the degradation mechanism of the self-heating effect,[19)] we assume that the reduction of interface state generation due to the vacuum cavity structure next to the gate oxide edges is another cause of the improved reliability of the GAA poly-Si TFTs with vacuum cavities under self-heating stress.

The degradation characteristics under dynamic stress are much closer to those under actual operating conditions than those under static stress during the application of circuits. Therefore, in addition to DC stress, the reliability of these GAA poly-Si TFTs with and without vacuum cavities under AC stress is also examined and compared. For the reliability test under dynamic stress, pulse trains are imposed on the gate electrode, and the drain and source are grounded. Rectangular pulse signals with a bias of −7.5 to +7.5 V, 50% duty ratio, and frequencies of 10 kHz, 100 kHz, and 1 MHz are adopted as AC stress. The rising time (t_r) and falling time (t_f) are both fixed at 5 ns. The dependence of I_{on} and V_{th} degradation on the stress time under AC stress is shown in Fig. 7. It has been reported that the degradation of poly-Si TFTs under AC stress is mainly caused by the increased number of trap states in the poly-Si channel induced by the hot carrier effect.[21,22)] Therefore, the GAA poly-Si TFTs with vacuum cavities exhibit much less I_{on} and V_{th} degradation than traditional ones owing to the greater equivalent gate oxide thickness near the drain edge, which reduces the lateral and vertical electric fields,[16,17)] thus

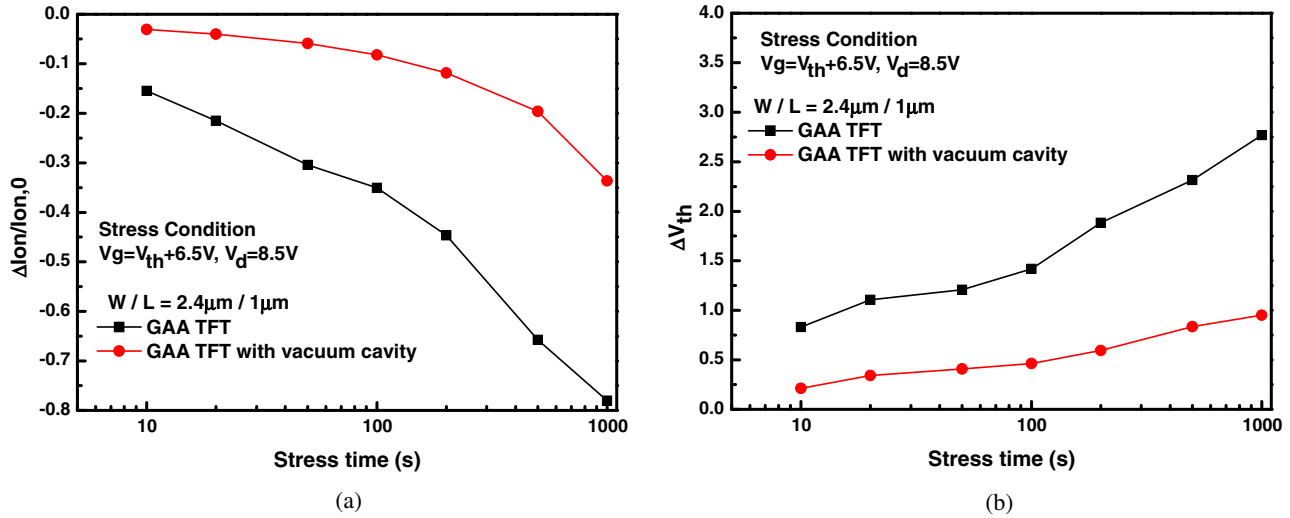


Fig. 6. (Color online) Dependence of (a) I_{on} and (b) V_{th} degradation on the stress time for the GAA poly-Si TFTs with/without vacuum cavities under self-heating stress condition.

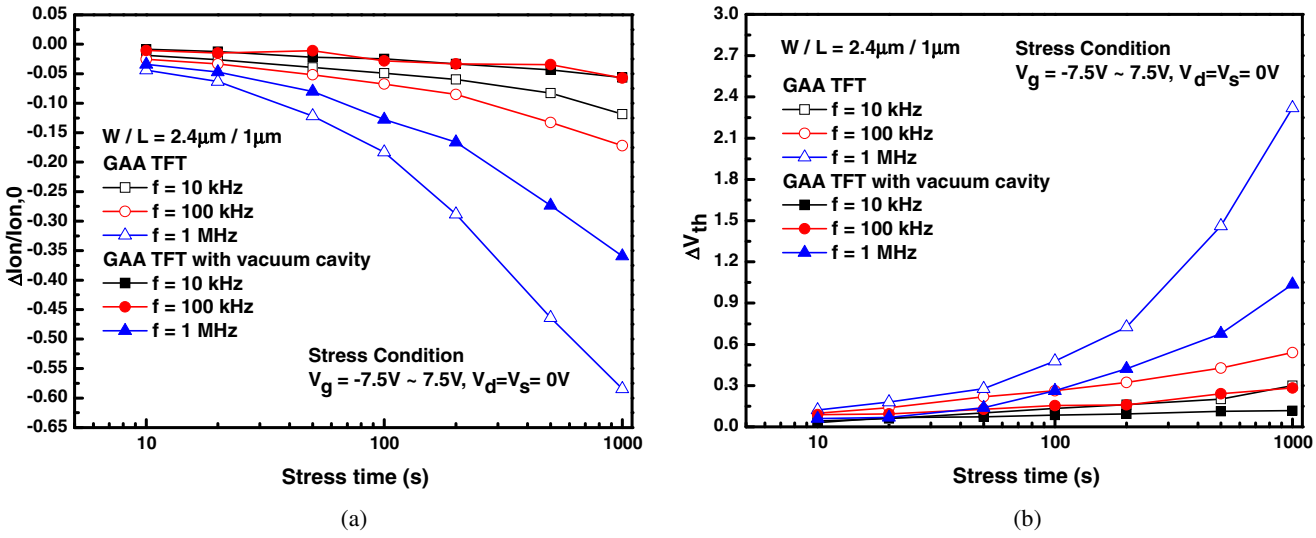


Fig. 7. (Color online) Dependence of (a) I_{on} and (b) V_{th} degradation on the stress time for the GAA poly-Si TFTs with/without vacuum cavities under dynamic stress condition.

reducing the hot carrier effect. It was observed that under the same stress time, taking the values of I_{on} or V_{th} degradation of traditional GAA poly-Si TFTs as a reference, the difference in $\Delta I_{on}/I_{on,0}$ or ΔV_{th} between the devices with and without vacuum cavities is increased with increasing AC stress frequency. The higher the AC stress frequency, the greater the improvement in the reliability of GAA poly-Si TFTs with vacuum cavities owing to the reduction of the vertical electric field near the drain edge by the vacuum cavity structure.

4. Conclusions

In this study, we propose GAA poly-Si TFTs with vacuum cavities around the edges of nanowire poly-Si channels, which are fabricated by spacer formation, partial wet etching of a gate oxide, and *in situ* vacuum encapsulation without any additional masks or advanced lithographic technology. Because of the completely surrounding gate structure and the increase in electric field by the spacer channel with three sharp corners, GAA poly-Si TFTs exhibit excellent electrical characteristics, resulting from the improvement of gate controllability in the short-channel TFTs. Moreover, GAA poly-Si TFTs with vacuum cavities next to the gate oxide edges exhibit further improved electrical properties, such as a reduced OFF-state leakage current while maintaining the on-current in the ON state, i.e., a higher ON/OFF current ratio, resulting from the vacuum cavity simultaneously serving as an offset region and an FID structure. Furthermore, regardless of whether static or dynamic electrical stress, the GAA poly-Si TFTs with vacuum cavities achieve superior reliability compared with the traditional ones. For GAA poly-Si TFTs with vacuum cavities, not only the electrical performance but also the reliability is significantly improved by the simultaneous reduction of lateral and vertical electric fields near the drain junction, resulting from the greater equivalent gate oxide thickness on the gate electrode edges.

Acknowledgements

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